Quality and Reliability

Report

FY 2017

Table of Contents

CHAPTER 1

Zilog's Quality Culture

Zilog's Quality Culture

RELIABILITY AND QUALITY ASSURANCE POLICY STATEMENT

Zilog's philosophy towards quality has been consistently aimed at continuous product improvement and optimization of processes associated with the design, manufacture, test and delivery of products that conform to all established requirements for total customer satisfaction.

It has been a Zilog tradition that the customer is the main driving force in a company-wide goal to achieve the highest quality possible. Through excellent management of its personnel, equipment, materials, environmental resources, and subcontractors Zilog is well positioned for success.

ZILOG QUALITY POLICY

zilog
An IXYS Company

QUALITY POLICY

Delight our Customers by…

- Doing the job right the first time
- Making and meeting commitments
- Excelling through planning and teamwork
- Driving continual improvement with Best Known Methods
- Respecting team members and making Zilog a great place to work

sdaley@zilog.com
Director of Quality and Reliability
Zilog - an IXYS Company

ZILOG'S QUALITY AND RELIABILITY PROGRAM

Zilog's Quality and Reliability Program is based on careful study of the principles laid down by such pioneers as W. E. Deming and J. M. Juran. Even more importantly, we have benefited from the observation and practical implementation of those principles as practiced in Japanese, European and American manufacturing facilities.

The Zilog program begins with employee involvement. Whether the judgment of our performance is based on perfection with incoming inspection, trouble free service in the field, or timely and accurate customer service, we recognize that our employees ultimately control these factors. Hence, our quality program is broadly shared throughout the organization.

Training

The integrity of our product design depends on the skills of our employees. Zilog training emphasizes the fundamentals involved in product design and processing for quality and reliability.

Customer Service, an important aspect of Zilog's quality performance as a vendor, also depends upon our people clearly understanding their jobs and our obligations to our customers. This aspect of training is also a part of the overall curriculum administered by Zilog.

Order Acknowledgment Policy

One definition of vendor quality performance is that the vendor "does what he or she promises or acknowledges." Acceptable reliability and quality is achieved only if Zilog and the customer are in agreement on product and delivery specifications.

Test Guardbanding

No physical attribute is absolute. Customers' test methods may differ from Zilog's due to variations in test equipment, temperature or specification interpretation. To ensure that every Zilog product performs to full customer expectations, Zilog uses a "waterfall" methodology in its testing. The first electrical tests made on the circuit for both AC and DC parameters, at the wafer probe operation, are guardbanded to the final test specifications. The final test specifications for both AC and DC parameters, in turn, are guardbanded to the quality control outgoing sample. The quality control outgoing sample is guardbanded to data sheet specifications. This technique of "waterfall" guardbanding eliminates circuits that may be marginal to the customer's expectations long before they get to the shipping container.

Product Characterization

Every Zilog product design is evaluated over extremes of operating temperature, supply voltage, and clock frequency prior to production release. This information permits the proper guardbanding of the test program waterfall and identification of any marginal "corners" in design tolerances.

A product characterization summary, which details the more important tolerances identified in the process of this exhaustive product design evaluation, is available to Zilog's customers.

Process Qualification

Zilog also qualifies every process prior to production by an exhaustive stress sequence performed on test chips and on representative products. Once a process regime is qualified, a process re-qualification is performed any time there is a major process change.

Product Qualification

In addition to characterization, every new Zilog product design is fully qualified by a comprehensive series of life, electrical, and environmental tests before release to production. Whenever possible, both industry standard environmental and life tests are employed. Again, a qualification summary is available to our customers that details certain key life and environmental data taken in the course of these evaluations. Please see Qualification Requirements for an example of the Zilog Package Qualification Summary and Device Qualification Summary.

PPM Measurement, Direct and Indirect

It is frequently said that if you want to improve something, you need to measure it. Therefore, Zilog measures its outgoing quality "parts per million" by the maintenance of careful records on the statistical sampling of production lots prepared for shipment. This information is then translated to a statement of our parts per million outgoing quality performance.

Of course, it is one thing for Zilog to think it is doing a good job in outgoing product quality and it is another for a customer to agree. Therefore, we ask certain key customers to provide us with their incoming inspection data that helps us calibrate our outgoing performance in terms of the actual results in the field. The fact that Zilog has been awarded "ship to stock" status by many customers testifies to our success in this area.

FIT Measurement Direct and Indirect

Just as Zilog records its outgoing quality in terms of parts per million, it also measures its outgoing product reliability in terms of "FITS" or Failures per billion device hours. This calculation is done by using the results of weekly operating life test measurements on the circuits performed in accordance with standard specifications.

Field Quality Engineers

Zilog maintains a force of skilled Field Application Engineers, who are also trained as Field Quality Engineers. These engineers are available on immediate call to consult our customers on any problems they may be experiencing with Zilog product performance.

Product Analysis

Product Analysis facilities, staffed by experienced professionals, exist at each Zilog site to provide rapid evaluation of in-process and in-field rejects. Zilog is pleased to share product analysis reports on specific products with the customer upon request.

Total Quality Program

Zilog employees actively participate in meetings where methods are proposed, reviewed, and adopted. These meetings enable a department to do its job in a more precise and accurate manner.

Environmental Protection Recycling

Zilog is committed to an environmental protection-recycling project that is becoming an international requirement. Zilog prefers that materials used to package its finished products be recyclable and/or manufactured from recycled material. The “Recyclable” symbol can already be found on shipping boxes, tubes and reels, and on shipping trays.

ZILOG ENVIRONMENTAL, HEALTH AND SAFETY POLICY

Zilog Environmental, Health and Safety Policy

Zilog's mission is to create superior value for our stakeholders. The health and safety of our employees, and the proper care of our environment based on the defined scope of the environmental management system are of paramount importance. Zilog's concern for them is not only good corporate citizenship, it's also good business. Zilog is committed to a continually improving Environmental, Health and Safety Management System. Strict compliance with applicable EHS regulations is considered a minimal standard – neither production goals nor financial objectives shall excuse noncompliance.

The core values of Zilog's EHS Management System are to:

- Create, maintain and promote a safe and healthful workplace for all employees.
- Comply with the intent as well as the letter of all applicable EHS regulations at the Federal, State, local levels, and other requirements to which Zilog subscribes.
- Set EHS goals and objectives and measure progress toward them.
- Promote a respect for the environment among employees.
- Conserve resources and minimize waste by reducing, reusing, and recycling.
- Integrate EHS considerations into business planning, decision making, and daily activities.
- Provide the resources and training to carry out this policy.
- Prevent accidents and minimize environmental impact.
- Communicate our EHS performance.
- Respond to the concerns of the communities in which we do business.
- Support EHS public policy development.
- Encourage our contractors and suppliers to adopt EHS standards similar to our own.
- Exchange EHS knowledge and technology.

These core values build on our tradition of quality, innovation, and continual improvement.

Alan Shaw
Vice President of Operations
Zilog, Inc.

ISO CERTIFICATION

Zilog is extremely proud to have received the following ISO 9001:2008 certification award, which reflect the stringent quality standards to which all Zilog products are manufactured.

FACILITY/LOCATION	*CERTIFICATION RECEIVED*
Zilog Electronics Philippines, Inc. (ZEPI) Manila, Philippines - Subcontractor Management, Assembly and Test of Power Devices, DCB Laser Scribe, Warehousing and Shipment	ISO9001:2008 BSI Management Systems

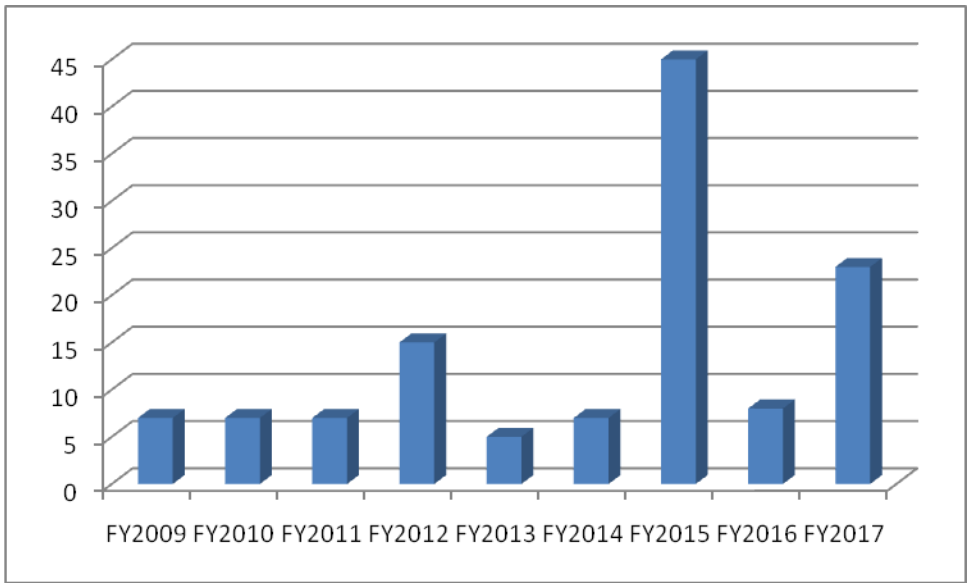
(*ISO - International Standards Organization)

ISO CERTIFICATION OF FOUNDRIES/SUBCONTRACTORS

FACILITY	*LOCATION*	*PROGRAM*
Wafer Foundries:		
UMC	Taiwan	ISO 9001/TS16949
TSMC	Taiwan	ISO 9001/TS16949
XFAB	USA	ISO 9001/TS16949
Assembly Subcontractors:		
UNISEM	Batam, Indonesia	ISO 9001/TS16949
Amkor	Manila, Korea	ISO 9001/TS16949
ASEK	Taiwan	ISO 9001/TS16949
UTL	Thailand	ISO 9001/TS16949
Greatek	Taiwan	ISO 9001/TS16949
LIKOM	Malaysia	ISO 9001
Test Subcontractors:		
Ardentec	Taiwan	ISO 9001/TS16949
ASET	Taiwan	ISO 9001/TS16949
Amkor	Manila, PI	ISO 9001/TS16949
UNISEM	Batam, Indonesia	ISO 9001/TS16949

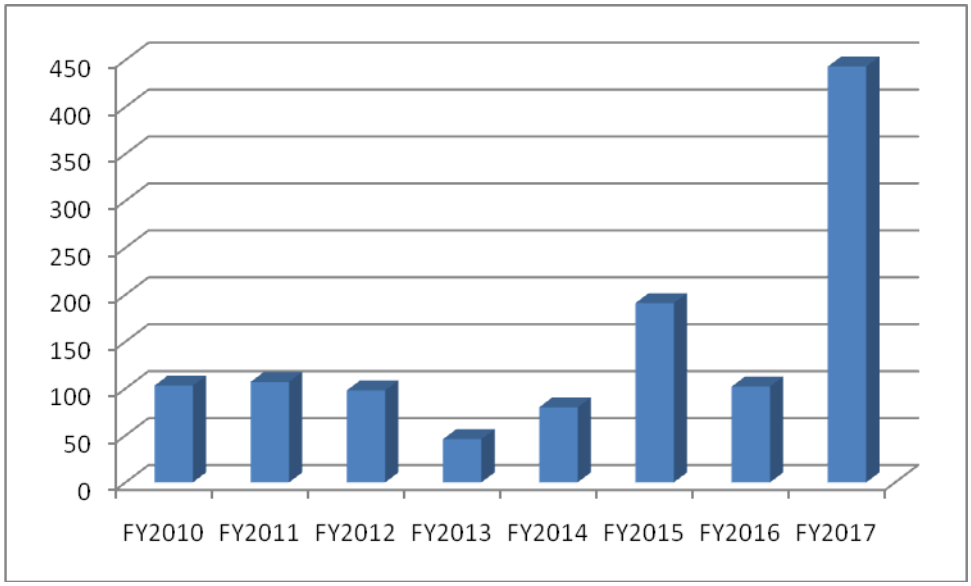
QUALITY AND RELIABILITY TREND CHARTS

Figure 1-1 – FIT Rate (FIT = Failure in Time: Failures per Billion Hours**)**



* No failure out of sample size

Figure 1-2 - PPM Electrical



CHAPTER 2

Customer Quality Support System

Customer Quality Support System

CUSTOMER FAILURE ANALYSIS/CORRELATION PROCEDURE

Zilog has a complete Customer Failure Analysis (CFA) system. Using this system, a customer may return units for failure analysis or test correlation. The sequence of events for the CFA procedure is as follows:

1. Customer suspects a failure.
2. The customer completes a CFA request. See Figure 2-1.
3. A CFA request is assigned a number for tracking.
4. The customer returns the unit(s) to the factory.
5. Product/Test Engineering performs a go/no-go electrical test.
6. The unit(s) and test results are given to the Failure Analysis Engineer.
7. If the unit(s) fail the test, the Failure Analysis Engineer performs electrical and physical analysis, and generates a CFA report.
8. If the unit(s) pass the test, the Failure Analysis Engineer generates a CFA report and returns the unit(s) to the customer.
9. Our goal is to provide a complete CFA report within 10 working days from the time the unit(s) are received.

Zilog and the customer will work together to reduce all types of failures to zero. The CFA procedure is one of several communication tools that can be used to achieve this goal, proving its overall effectiveness since its inception in 1985.

Figure 2-1

CFA Request-Failure Analysis Questionnaire Form

Purpose: To eliminate time spent researching a failed component/part history in order to concentrate on finding the root cause of failure or complaint by the customer

FAILURE ANALYSIS QUESTIONNAIRE

ZiLOG Confidential | SOP0929-Form1 Page 1 of 1 | Revision 07

GENERAL INFORMATION:

Initiated By: _____ Date: _____ B.U.: _____

Customer Name: _____

Customer Address: _____

Phone No: _____ Are Parts Under Warranty? ☐ Yes ☐ No

NOTE: ***Failure analysis of out of warranty parts is for information only.***

PART INDENTITY:

Device: _____ Date/bb Code: _____ Total # devices in lot: _____

Qty. devices tested/inspected: ___ Qty. being returned: _____ Qty. of failed devices: _____

Customer Application: _____

FAILURE DESCRIPTION:

Incoming: _____ Assembly: _____ Final Test: _____ Field Return: _____

Low Noise Option? ☐ Yes ☐ No How long in service before failure occurred? _____

Was part removed with any other parts? ☐ Yes ☐ No _____

Did failure follow part? ☐ Yes ☐ No _____

Additional processing temperatures which part had seen before failure occurred: _____

Is this a new application for this device? ☐ Yes ☐ No _____

Is this a new failure mode? ☐ Yes ☐ No _____

Is there a Customer board or test program available for use at ZiLOG? ☐ Yes ☐ No

Are there failing and passing samples available for correlation work? ☐ Yes ☐ No

Process steps part had seen up to time of failure:

OTP RETURNS:

Programmer used: _____ Software Rev: _____ Checksum: _____

Option Bits Selected: _____

NOTE: *For the most thorough analysis, please include a Hex file of the Customer's code.*

ADDITIONAL DETAILS:

Table 2-2
Summary of QC Test Equipment

Equipment At ZEPI	Brand	Usage
ISOMET Low Speed Saw	Buehler	Cross-Section Analysis
Curve Tracer	Tektronix 576/370B/577	Bench Check
ESD Tester	IMCS 700	VZAP Testing
Polimet Polisher	Buehler	Cross-Section Analysis
High Power Scope	Olympus	External/Internal Visual Inspection
Low Power Scope	Olympus / ABCELLON Western Dynamics	External/Internal Visual Inspection
Decapper	PS102W	Decapping of Plastic Devices
Hot Plates	3D Ready-Heat / Lab Companion	Solderability-Steam Aging
Pressure Cooker	Electric Steroclave	Reliability Test
SEM & EDX	Leica S420	Visual & Elemental Analysis
Digital Multimeter	Fluke	Latchup Test
Timer	Gralab	Timed Operations
Profile Projector	Mitutoyo	Dimensional Inspection
Temp Cycle (TSE 11A)	Escpec	Temperature Cyling
Mechanical Shock Tester	Lansmont	Mechanical Shock Test
VVF Test	Unholtz-Dickie	VVF Test
Thermal Shock	Tabai	Thermal Shock Test
Beam Balance	None	Weight Measurement
Digital Linear Gauge	---	Wafer Thickness Check (IQC)
High Power Microscope w/Video Camera	RCA/Nikon Optiphot 200	Wafer Level Inspection
Ion Coater	Eiko Engineering	SEM Sample Preparation
Solder Pot	ESICO	Solderability Test
Convection Reflow Oven	ESSEMTEC	Package Reflow
Ultrasonic Cleaner	Branson 1510	Die cleaning

Table 2-2
Summary of QC Test Equipment (cont'd)

Equipment At Meridian	Brand	Usage
Gold Coater	Cressington	SEM Sample Prep (Backup)
Low-Speed Diamond Saw	Buehler	Package Cross
Bench Top Furnace	Lindberg	High Temp Analysis to 1100C
High Temperature Ovens:		
175C	Blue M	Bake Recovering
125C	Blue M	SEM Sample Storage
Exhaust Hood	Kewaunee	Chemical Use Safety
Wet Sink w/Exhaust	JST Plastics	Chemical Use Safety
Hot Plate PC100	Corning	Wafer Reliability Analysis
Hot Plate PC100	Corning	Hot Chemical Etch
Hot Plate	Lindberg	Wafer Pressure Pot Test
Hot Plate	Corning	Chip Unzip
Ultrasonic Cleaner (2)	Bransonic	Sample Cleaning
Etch Automated Dual Acid Decapsulator	Elite Etch	Part Decapsulation
Timers (2)	Gralab	Timed Operations
Dial-O-Gram (2)	Ohaus	Chemical Measurement
Curve Tracer 576	Tektronix	Bench Check
Curve Tracer 577	Tektronix	Bench Check
Temperature Forcing Unit	Temptronic	Bench Temperature Testing
Laser Cutter	New Wave EZ LAZE	Trace Cutting
FIB With SIMS (SIMS not working)	FEI	Micro Cross Sectioning, Device Modification and Elemental Analysis and Imaging
Reactive ION Etcher (REI), 8-Inch	Trion	Device Deprocessing
Polycon, BF, DF, DIC, Confocal, Fluorescence,	Leica-Reichert	Product Visual Examination
W/8x8" Stage	Semprex	Feature Size Measurement
Visionary 2000	Hypervision	Emission Microscope,
Multiprep	Allied High Tech	Parallel Polishing
5x - 100x Optical Microscope	Nikon Eclipse L200	Bright field, Dark field, Numarsky, Confocal inspection, Digital Camera1280 x 1944
High Temperature Oven 20 C - 550 C	Grieve	Hammer Testing, Ink Dot Curing

Table 2-2
Summary of QC Test Equipment (cont'd)

Equipment At Meridian	Brand	Usage
4156B Precision Semiconductor Parameter Analyzer	HP	Parametric Tester
4274A Multi-Frequency LCR Meter	HP	Tester (Inductance, capacitance, resistance instrument)
Microminipulator Test Station (2)	Micromanipulator	Probe Test
Philips XL30	Philips	Ultra High Resolution
SFEG SEM		SEI, BSE (Solid State)
SMZ-10 Stereo Scope	Nikon	External/Internal Visual Inspection
XT2-90 XRAY System	Matrix Focal Spot	Internal Assembly, wire bonding, and solder void inspection
Equipment At Milpitas		
Spectrum Analyzer	HP-8591A	Near Field EMI Testing
Pre-Amplifier	HP8447D	Near Field EMI Testing

USE OF OUTSIDE FMA LABS

Charles Evans & Assoc.
301 Chesapeake Drive
Redwood City, CA 94063

Integrated Service Technology Inc.
No. 19, Puding Rd., East District
Hsinchu City 300, Taiwan (R.O.C)

CUSTOMER NOTIFICATION SYSTEM

Customer Service notifies the customer with a formal change notification letter on major process and design changes. The following is a list of criteria for which all customers are notified:

- Changes to form, fit or function
- Changes to product design and manufacturing locations
- Changes to manufacturing Processes and/or materials
- Changes that may affect product quality, reliability or manufacturability

Customers will be provided with change notification letter that gives the customer a schedule of the conversion, stating that:

The customer will be given 30 days to request qualification samples from Zilog.

New product will be shipped within 60 days from the date of the letter, unless Zilog receives written notice from the customer to continue shipping their current qualified product.

For automotive customers, change notification may be accompanied by a submission of a Product Submission Warrant (PSW) and the necessary attachments (Part Drawing, Failure Mode and Effects Analysis, Engineering Samples) depending if the customer requests that the PPAP process be initiated.

New products for automotive customers will require a PPAP Level 3 Process.

CHAPTER 3

Qualification Requirements

Qualification Requirements

Product/Process Qualification Requirements

Per Procedures SOP0940 and SOP0909, Zilog performs initial qualification on new processes, changes on existing process, new product and changes on existing package following requirements of Table 3-1. Re-qualification is required when material changes occur.

Table 3- 1
Product/Process Qualification Requirements

PROCESS AND PRODUCT QUALIFICATION REQUIREMENTS

TEST	TEST METHOD	CONDITIONS	READPOINTS	QUALIFICATIION READPOINT	ACC/SS
ESD-HBM(3)	JESD22-A114 current revision	Per Test	N/A	N/A	2000V Min
ESD-CDM	JESD22-C101	Per Test	N/A	N/A	Per classification
LATCH-UP(3)	JESD78 current revision	Per Test	N/A	N/A	0/6 @ 200mA min
LIFE TEST	MIL-STD-883 Method 1005.8	Condition B, 150°C	N/A	184 hours	0/77
LIFE TEST(1)	MIL-STD-883 Method 1005.8	Condition B, 125°C	500 & 1000 hours	1000 Hours***	0/77
TEMPERATURE CYCLE	JESD22-A104	Condition C	N/A	500 Cycles	0/45
PRESSURE POT (Autoclave)	JESD22-A102	121°C/15 PSIG	N/A	96 hours	0/45
HAST	JESD22-A110	130°C/85%	N/A	96 Hours	0/45
FLASH Endurance Test	JESD22-A117	Full specified temp range (min, RT, max temp).	N/A	Min. # of specified cycles (typ. 10,000 Cycles)	0/77 per temp range
High Temperature Storage(2)	MIL-STD-883 Method 1008.2	150°C	500 & 1000 Hours	1000 Hours (2)	0/45
Flash Data Retention (5)	JESD22-A117	150°C	500 and 1000 hours (168 opt.)	1000 Hours	0/77
MSL Preconditioning (4)	J-STD-022-A113	Per Test	N/A	N/A	

(1) Products that contain FLASH memory must be life tested at 125°C.
(2) This stress is only required for process monitors and qualification of new OTP processes. Devices will be programmed with the checkerboard program, verified and then programmed with inverse checkerboard to program the entire array. Conditional Qualification may be granted for products that require 150ºC at 500-hour readout.
(3) The test method originally used to qualify a product may be used if the product is transferred to a different Fab
(4) Preconditioning is required for Temp Cycle, HAST, and PPOT.
SOIC/SSOP are rated as MSL 1
PLCC/QFP/LQFP/BGA/QFN(ELP) are rated as MSL 3
(5) This stress is only required for qualification of new flash processes or automotive qualification. QA and product engineering will determine if endurance pre-cycling will be required prior to data retention.

Qualification of new package may require all tests requirements on Table 3-2. A package that has been qualified at one of Zilog's assembly subcontractors is considered to be a new package when run at a different assembly subcontractor. Changes to an existing package may require all the tests listed in Table 3.2.

Table 3- 2
Package Qualification Requirements

PACKAGE QUALIFICATION REQUIREMENTS

TEST	TEST METHOD	CONDITIONS	READPOINTS	QUALIFICATION READPOINT	ACC/SS
LIFE TEST **	MIL-STD-883 Method 1005.8	Condition B, 125°C	168 hours	168 hours	0/77
TEMPERATURE CYCLE	JESD22-A104	Condition C	N/A	500 Cycles	0/45
PRESSURE POT	JESD22-A102	121°C/15 PSIG	N/A	168 Hours	0/45
HAST ***	JESD22-A110	130°C/85%	96 Hours	96 Hours	0/45
BOND STRENGTH	MIL-STD-883 Method 2011.7	Condition D	N/A	N/A	0/10 wires
BALL SHEAR	JESD22-B116 current revision	Per Test Method	N/A	N/A	0/3 wires
DIE SHEAR	MIL-STD-883 Method 2019.7	Per Test Method	N/A	N/A	0/1
PHYSICAL DIM.	MIL-STD-883 Method 2016	Per Test Method	N/A	N/A	0/5
LEAD FATIGUE	MIL-STD-883 Method 2004.5 and JESD22-B105	Per Test Method	N/A	N/A	0/1
SOLDERABILITY *	MIL-STD-883 Method 2003.8	Per Test Method	N/A	N/A	0/6
X-RAY	MIL-STD-883 Method 2012.7	Per Test Method	N/A	N/A	0/32
High Temperature Storage	MIL-STD-883 Method 1008.2	150°C	168 hours	168 hours	0/77
MSL Test/Preconditioning ****	J-STD-022-A113	Per Test	N/A	N/A	
External Visual	MIL-STD-883 Method 2009.9	N/A	N/A	N/A	0/125

***** Use 260ºC for green package.
** Load samples at High Temperature Storage if there is no available burn-in board.
*** Could be omitted if there is no available board.
******** Pre-conditioning is required for Temp Cycle, HAST and PPOT.
SOIC/SSOP are rated as MSL 1
PLCC/QFP/LQFP/BGA/QFN are rated as MSL 3

Zilog Package Qualification Summary

PACKAGE QUALIFICATION SUMMARY
ZiLOG Authorized Distribution

Document Control #: QR-9459 Rev.: 01
Page 1 of 1 OP25

		DATE:	02-08-2006
PRODUCT:	Z86E0412SEGR538PTR (GREEN Package)	**PROCESS:**	X5220
WRITTEN BY:	Glenn Escano	**APPROVED:**	Malie Fonte

- **INTRODUCTION**

This report summarizes the qualification results of the Green Package for Delphi Mechatronics. The green package version is compliant to the E.U. RoHS directive.

- **INFORMATION SUMMARY**

All qualification tests were performed to MIL-STD-883, JEDEC and/or internal ZiLOG procedures.

PRODUCT QUALIFICATION

Test Description	Test Method	Condition	Test Result
Temperature cycle	MIL-STD-883/1010	Condition C	0/45, 500 cycles
Pressure Pot	120 °C, 15 PSI	Per Test	0/45, 168 hours
Package Integrity	240 °C, 10 seconds	Per Test	0/15
High Temp Storage	150 °C	Per Test	0/77, 168 hours
MSL Classification	Level 1	Per Test	0/22
Burn-in	125 °C	Per Test	0/77, 168 hours
Tin Whisker Test	Room temperature	Per Test	Passed, 24 months
Tin Whisker Test	Dry bake @ 50-55 °C	Per Test	Passed, 30 months
Tin Whisker Test	85 °C /85% RH	Per Test	Passed, 18 weeks
Tin Whisker Test	30 °C /60% RH	Per Test	Passed, 48 weeks
Tin Whisker Test	Temp Cycle -65 to 150°C	Per Test	Passed, 1000 cycles

QUALIFICATION	TYPE	DOC. NO.
Package	Leadfree (Pure Tin) and Green Compound Qualification	ZQR-3062067B
Device	Z86E0412SEGR538PTR Green Package Qualification Report	QR-9450

ZILOG, Inc. 532 Race Street, San Jose, CA 95126 (T) 408-558-8500

CHAPTER 4

Quality Monitor Systems

Quality Monitor Systems

FAILURE RATE PREDICTION CALCULATIONS

Zilog estimates the operating life of our products through statistical methods. It is not possible to guarantee the lifetime of an individual part because the tests to determine this are destructive. Therefore, we can only use statistics to predict the typical behavior of groups of parts. These predictions, and the methods they are based on, are documented in FIT reports. The FIT report is based on process specific data and is derated to reflect individual device characteristics. FIT reports are available for all of Zilog's products.

Other factors that affect device lifetime include actual operating hours, ambient temperature, stability of the power supply, board assembly and other handling practices. All of these factors are outside of the control of Zilog and may dramatically shorten the lifetime of a device.

The failure rate for each product and process is a function of time, temperature and applied power. The primary temperature is, of course, the product junction temperature. This is externally influenced by the ambient temperature and internally influenced by the power dissipated in the die. The power dissipation, in turn, is a function of the duty cycle and applied VCC. In the case of CMOS, product power dissipation is also a function of the operating frequency. Zilog product failure rates were derived from accelerated life test results accumulated on an ongoing basis as part of the Zilog reliability monitor. The accelerated life test reliability data includes both infant mortality (early life results 0-160 hours) and long term life results (168-1000 hours). Various interim time points and sample sizes are used. Life test may be performed at either 125°C for 1000 hours or the Mil Std 883 equivalent or 150°C for 184 hours.

FIT Rate Calculation

The acceleration obtained when using high temperature life stressing may be calculated for various stress and application temperatures using the widely accepted Arrhenius equation as follows:

$$A = e^{\frac{-E_a(T_1-T_2)}{kT_1T_2}}$$

Where:

A = Acceleration factor (dimensionless)
E_a = Activation energy (eV)
T_1 = Application junction temperature (K)
T_2 = Stress junction temperature (K)
k = Boltzmann Constant 8.617 x 10^{-5} (eV/K)

Assume E_a = 0.7 eV, application ambient temperature T_a = 55°C, and stress ambient temperature T_s = 125°C. Consider a typical CMOS product Z84C00 operating with a 100% duty cycle at 8 MHz in a 40 pin PDIP package. With V_{CC} = 5.0 V, I_{CC} = 40 mA, and package thermal resistance θ_{JA} = 43°C/W the application junction temperature

$$T_1 = T_a + V_{CC}I_{CC}\theta_{JA} + 273.15$$

and the stress junction temperature

$$T_2 = T_s + V_{CC}I_{CC}\theta_{JA} + 273.15$$

yielding T_1 = 336.75 K and T_2 = 406.75 K. Substituting these values into the above Arrhenius equation gives the acceleration factor

A = exp {-0.7(336.75 - 406.75)/[8.617 x 10^{-5} (336.75)(406.75)]} = 63.53

So 1000 hours of life stress at 125°C is equivalent to 63,530 hours of system application operation at 55°C.

FIT and Failure Rate Estimation:

The High Temperature Operating Life (HTOL) stress result is 0 rejects after 561,404 device hours at 125°C. Failure rate estimations are made assuming a Poisson distribution using the χ^2 density function to assign confidence values as an estimate for the general population as follows:

60% Confidence # Fails = 0 then χ^2 = 1.85

Given 0 rejects from 561,404 device hours at 125°C, using χ^2 gives a median failure rate of 1.85/2 rejects per 561,404 device hours or 1.648 reject per 10^6 device hours.

Failure rate = 1.648/10^6 device hrs. = 1648 rejects/10^9 device hrs.
= 1648 FIT at 125°C
Failure rate = 1648/63.53 = 25.94 FIT at 55°C (A = 63.53 as calculated above)

MTBF = (10^9/25.94)/(24*365) = 4401 years

ESD TESTING METHODOLOGY

Zilog has an unqualified commitment to quality and reliability and, as part of this commitment; Zilog strives to provide the best possible ESD protection for each of our products.

Since 1983, Zilog has had an ongoing electrostatic discharge development program to monitor and improve its ESD protection circuitry. During an ESD event, the ESD protection circuitry must absorb the power of the ESD pulse while allowing little or no damage to occur to the internal circuitry of the chip. A 3000 volt ESD pulse can induce transient currents approaching one amp, and it is the management of these transient currents that is the key to good ESD protection. At Zilog, ESD protection circuits have been developed to optimize the handling of ESD pulse currents, by paying close attention to current flow patterns, and minimizing current density and crowding problems that cause damage to the circuitry.

All of Zilog's products are tested for their ESD immunity as part of routine internal qualification procedures. The ESD test hardware is in compliance with JEDEC JESD22-A1214B Human Body Model.

LATCHUP TESTING METHODOLOGY

Zilog has an unqualified commitment to quality and reliability and, as part of this commitment, also strives to provide each of its products with the best possible latchup protection.

Latchup may occur as a result of either current injection (positive or negative) or supply pin over voltage. The latchup action is that of a parasitic SCR, converting from a high-impedance state, to a low impedance, regenerative, state. The resulting current flow may exceed the design capabilities of the device. Damage may occur to interconnections (bond wires and die metallization) as a result of thermal heating effects and excessive current flow. During conditions which may lead to latchup, the device must be able to shunt the triggering event (the positive or negative injection current) without damage to the device. All of Zilog's products are tested for their latchup immunity per JESD 78 as part of our routine qualification procedure.

ZILOG'S RELIABILITY SUMMARY

The tests currently employed under Zilog's reliability monitor include early life (burn-in), steam pressure pot, and temperature cycle.

In addition, a long-term life test is performed on selected lots to gather FIT data. Following are brief descriptions of various reliability tests included in this program.

EARLY LIFE

Early Life testing, also called burn-in, is typically performed at 125°C for 168 hours. A dynamic or static bias is employed, depending on the device that is being tested. Early Life test results expose process or assembly defects. These results are a valuable measure of a given fabrication or assembly process.

LONG TERM LIFE

Long Term Life testing is generally performed at 150°C for 184 hours or 125°C for 1000 hours. Either dynamic or static bias is used to stress the device appropriately. These test results are used to estimate field operation lifetime for a device. This data can be applied to all products manufactured using the same fabrication process

PRESSURE POT

Pressure pot testing is performed at 121°C, 15 PSIG, and 100% relative humidity. This test evaluates the ability of a plastic device to withstand the long-term effects of a humid environment.

TEMPERATURE CYCLE

Temperature Cycle testing is performed at a –65°C to 150°C temperature. This test uses an air-to-air environment. The 215°C cold to hot temperature difference determines if proper thermal expansion matching exists between all materials used in device manufacture. The temperature cycle simulates the thermal stresses a device undergoes during power-up and power-down events.

HIGHLY ACCELERATED STRESS TEST

The Highly Accelerated Stress Test (HAST) is performed at a 141°C temperature and 85% Relative Humidity (RH) at 2 ATM of pressure with alternate pin bias. This test replaces the traditional 85/85 test and greatly reduces the time taken to evaluate the ability of a plastic encapsulated device to withstand the long-term effects of a biased humid environment.

PACKAGE INTEGRITY TEST

Package Integrity testing ensures the integrity of surface mount devices in terms of package cracking, bonding craters, and marked deterioration as a result of heat application during the soldering operation. This includes testing of 5 units on each 3 legs as follows:

CONTROL	-	10-SECOND SOLDER DUNK AT 240°C
TEST 1	-	10-HOUR *PPT
		10-SECOND SOLDER DUNK AT 240°C
TEST 2	-	10-HOUR *PPT
		3-HOUR OVEN BAKE AT 150°C
		10-SECOND SOLDER DUNK AT 240°C

(*PPT = Pressure Pot Testing at 121°C, 100% RH, 2 ATM)

End-points are room temperature electrical test, visual inspection, mark permanency and crater test. Solder dunk temperature is 260°C for Green Package (G parts, RoHS)

Table 4-1

ZILOG RELIABILITY MONITOR TESTING REQUIREMENTS					
TEST	SAMPLE SELECTION	FREQUENCY	SAMPLE SIZE	ALLOWABLE REJECTS	TEST CONDITION
Temp Cycle or	Each pkg type per subcon	Every six months	45	0	-65ºC +0/-10 to 150ºC +15/-0, , 500, 1000 cycles
Thermal Shock**	Each pkg type per subcon	Every six months	45	0	-55ºC +0/-10 to 125ºC +10/-0
Pressure Pot	Each fab process and each pkg type per subcon	Every six months	45	0	168 & 336 hrs, 121ºC, 100% RH, 2 ATM
Burn-in Life Test*	Per FAB Process	Every three months	77	0	160 +8/-0 hrs, 125ºC or 184 hrs, 150ºC
	NMOS/CMOS	Every two months	77	0	1000 hrs, cum 125ºC or 184 hrs, 150ºC
Package Integrity	PLCC/QFP, LQFP, , SOIC, SSOP, QFN per subcon	Every two months	15	0	Per SOP1656
ESD	Each new die rev/device	N/A	9 units minimum	N/A	Per JESD22-A114
Latch up CMOS	Each new die rev/device	N/A	6 units minimum	N/A	Per JESD78
Solderability	Each pkg type per subcon	Monthly	6	0	Mil Std 883
Lead Fatigue Test	Each pkg type per subcon	Monthly	1 dummy unit	0	SOP1662
DCB Roughness Test	Per plating subcon	Quarterly	5 dummy singulated pieces	0	SOP2244
DCB Solderability Test	For plated - Per plating subcon and assembly For un-plated - Per assembly Subcon	Quarterly	6 dummy singulated pieces	0	SOP2244
DCB Bondability Test	For plated - Per plating subcon and assembly For un-plated - Per assembly Subcon	Quarterly	2 dummy singulated pieces	0	SOP2244

Products that contain FLASH memory require 125C, 1000hrs Burn-in and can be conditionally released after 500hrs.

** Thermal shock could be omitted if sampling is done at Temp Cycle.

Table 4-2

Burn In Life Test

DEVICE	LOT NUMBER	PLATE 1	FAB PROCESS	REJ/SS	CONDITION
S3F80P5XZZ-LM85	K8D9713F	S3F80P5	0.13um. 2P 5M	0/80	125ºC/832HRS
Z8S18020FEG	EAGT7163CPA	Z8S180PB	X6120	0/77	150°C/184HRS
Z8S18020FEG	EAGT7163PA	Z8S180PB	X6120	0/77	150°C/184HRS
Z8018010FSG	AGT72172QQQE	Z80180HA	X4110	0/80	150°C/184HRS
S3F80RBXZZ-KZ8B-2250	G4308B015	S3F80RBAB	0.11um Eflash 4P 5M	0/77	125°C/500HRS
Z8F042ASJ020SG2156	AACBH147.00E.A	8F042ACA	TSMC	0/77	125°C/168HRS
Z8F022APB020SG	AACFN043.00QQQA.A	8F042SAB	TSMC	0/77	125°C/168HRS
Z84C0006PEG	AGT75258PE	Z84C00HB	X4120	0/77	150°C/184HRS
Z16C0210VSG	AT80215A.A	Z16C04BB	X4120	0/77	150°C/184HRS

Table 4-3

Pressure Pot Test, 121°C, 2 ATM

PRESSURE POT				
FAB PROCESS	DEVICE	LOT #	DIE STEP	168 HRS
ASSY LOC: UNISEM-BATAM				
X5221	Z8927320VSG	AAT74867HS.A	Z89373CC	0/45
X3120	Z84C2006VEG	AAT69318QPAA.A	Z84C20BB	0/45
X5220	Z86E3016SSG	AT727024HQQQB.A	Z86E40DG	0/45
UMC 0.35um 2P4M	Z8F1232HJ020SG	AAR5SSMQQQB.A	8F0830AC	0/45
X5220	Z86E4412ASG	AAT74339HPE.A	Z86E44AF	0/45
TSMC 0.35um	Z8FS040BSB20EG	AACGF295.00G.A	8F042SAB	0/45
TSMC 0.35um	Z8F022APB020SG	AACFN043.00QQQA.A	8F042SAB	0/45
X5220	Z86E4412ASK	AEAT75256HPQQ2.A	Z86E44AF	0/45
X5220	Z86E4412ASG	AEAT75256HPQQ1.A	Z86E44AF	0/45
TSMC	Z8F1681QN024XK2247	AAW3S725.00A.A	8F6482AC	0/45
X4120	Z16C0210VSG	AT80215A.A	Z16C04BB	0/45
ASSY LOC: AMKOR				
X5221	Z86E8316VEG	ABT66209HQQQQQPA	Z86E83BC	0/45
X5120	Z8038018FSG	ABT51936QQQA	Z80380CD	0/45
TSMC	Z8F0411PH020SG	ABCCY982.00IPA	Z8F082BE	0/45
TSMC 0.35 um 2P 4M	Z16F2811AL020EG	ABCAF897.00QRC	8F1285AB	0/45
ASSY LOC: GREATEK				
X4120	Z84C0006PEG	AGT75258PE	Z84C00HB	0/45
X4120	Z84C0010AEG	AGT75258QPC	Z84C00HB	0/45
X4110	Z8018010FSG	AGT72172QQQE	Z80180HA	0/45
ASSY LOC: NANTONG				
0.13um, 2P 5M	S3F8S19XZZ-ER89	603Y8Y5	S3F8S19XZZ-W	0/45
PSTS				
0.11um 4P 5M	S3F80RBXZZ-KZ8B-2250	G4308B015	S3F80RBAB	0/45
0.13um, 2P 5M	S3F8S7BXZZ-TW8B	603T9Y405	S3F8S7BXZZ-W	0/45
0.13um, 2P 5M	S3F8S7BXZZ-TW8B	603T9Y406	S3F8S7BXZZ-W	0/45
0.13um, 2P 5M	S3F8S6BXZZ-QT8B	603UPP105	S3F8S6BXZZ-W	0/45
0.13um, 2P 5M	S3F8S6BXZZ-QT8B	603UPP104	S3F8S6BXZZ-W	0/45

Table 4-4

Temperature/Humidity Test

TEMP/HUMIDITY TEST				
ASSY LOC	**DEVICE**	**LOT #**	**DIE REV**	**RESULT**
AMKOR				
TSMC 0.35u	Z16F2811AL20EG	ABCAF897.00QRC	8F1285AB	0/22
X5221	Z86E8316VEG	ABT66209HQQQQQPA	Z86E83BC	0/22
UNISEM-BATAM				
X5221	Z8927320VSG	AAT74867HS.A	Z89373CC	0/112
X5220	Z86E4412ASK	AEAT75256HPQQ2.A	Z86E44AF	0/135
X5220	Z86E4412ASG	AEAT75256HPQQ1.A	Z86E44AF	0/135
X4120	Z16C0210VSG	AT80215A.A	Z16C04BB	0/140
TSMC 0.35u	Z8FS040BSB20EG	AACGF295.00G.A	8F042SAB	0/22
X3120	Z84C2006VEG	AAT69318QPAA.A	Z84C20BB	0/22
GREATEK				
X4110	Z8018010FSG	AGT72172QQQE	Z80180HA	0/22
X4110	Z8018010FSG	AGT72172QQQE	Z80180HA	0/22
NANTONG				
0.13um, 2P 5M	S3F8S19XZZ-ER89	603Y8Y5	S3F8S19XZZ-	0/140
PSTS				
0.11um 4P 5M	S3F80RBXZZ-KZ8B-2249	A66514804V	S3F80RBAA	0/140
0.11um 4P 5M	S3F80RBXZZ-KZ8B-2250	G4308B015	S3F80RBAB	0/45
0.13um, 2P 5M	S3F8S7BXZZ-TW8B	603T9Y405	S3F8S7BXZZ-	0/22

Table 4-5
Temperature Cycling Test, Condition C, -65°C To 150°C

TEMP CYCLE, TEST COND C.					
ASSY LOC	**DEVICE**	**LOT #**	**DIE STEP**	**500X**	**1000X**
UNISEM-BATAM					
X5221	Z8927320VSG	AAT74867HS.A	Z89373CC	0/45	-
X3120	Z84C2006VEG	AAT69318QPAA.A	Z84C20BB	0/45	-
X5220	Z86E3016SSG	AT727024HQQQB.A	Z86E40DG	0/45	-
UMC 0.35um 2P4M	Z8F1232HJ020SG	AAR5SSMQQQB.A	8F0830AC	0/45	-
TSMC	EZ80F91NAA50SG	AACGV720.00QQQB.A	Z80F91BC	0/45	-
X5220	Z86E4412ASG	AAT74339HPE.A	Z86E44AF	0/45	-
TSMC 0.35um	Z8FS040BSB20EG	AACGF295.00G.A	8F042SAB	0/45	-
TSMC 0.35um	Z8F022APB020SG	AACFN043.00QQQA.A	8F042SAB	0/45	-
X5220	Z86E4412ASK	AEAT75256HPQQ2.A	Z86E44AF	0/45	0/45
X5220	Z86E4412ASG	AEAT75256HPQQ1.A	Z86E44AF	0/45	0/45
TSMC	Z8F1681QN024XK2247	AAW3S725.00A.A	8F6482AC	0/45	
X4120	Z16C0210VSG	AT80215A.A	Z16C04BB	0/45	-
AMKOR					
X5221	Z86E8316VEG	ABT66209HQQQQQPA	Z86E83BC	0/45	-
X5120	Z8038018FSG	ABT51936QQQA	Z80380CD	0/45	-
TSMC	Z8F0411PH020SG	ABCCY982.00IPA	Z8F082BE	0/45	-
TSMC 0.35 um 2P 4M	Z16F2811AL020EG	ABCAF897.00QRC	8F1285AB	0/45	-
GREATEK					
X4120	Z84C0010AEG	AGT75258QPC	Z84C00HB	0/45	-
X4110	Z8018010FSG	AGT72172QQQE	Z80180HA	0/45	-
X4120	Z84C0006PEG	AGT75258PE	Z84C00HB	0/45	-
NANTONG					
0.13um, 2P 5M Emb Fla	S3F8S19XZZ-ER89	603Y8Y5	S3F8S19XZZ-V	0/45	-
PSTS					
0.13um, 2P 5M Emb Fla	S3F80RBXZZ-KZ8B-2249	A66514804B	S3F80RBAA	0/45	
0.13um, 2P 5M Emb Fla	S3F8S7BXZZ-TW8B	603T9Y405	S3F8S7BXZZ-V	0/45	-
0.13um, 2P 5M Emb Fla	S3F8S7BXZZ-TW8B	603T9Y406	S3F8S7BXZZ-V	0/45	-

Table 4-6

Highly Accelerated Stress Test (HAST), 140°C , 85% RH, At 2 ATM

HAST				
ASSY LOC	**DEVICE**	**LOT #**	**DIE REV**	**96 HRS**
UNISEM-BATAM				
UMC 0.35u 2P4M	Z8F1232HJ020SG	AAR5SSMQQQB.A	8F0830AC	0/45
X5220	Z86E4412ASG	AAT74339HPE.A	Z86E44AF	0/45
X3120	Z84C2006VEG	AAT69318QPAA.A	Z84C20BB	0/45
TSMC 0.35u 2P4M	EZ80F91NAA50SG	AACGV720.00QQQB.A	Z80F91BC	0/45
X4120	Z16C0210VSG	AT80215A.A	Z16C04BB	0/45
UMC 0.35u	Z8F1232HJ020SG	AAR5SSMQQQB.A	8F0830AC	0/45
TSMC 0.35u	Z8FS040BSB20EG	AACGF295.00G.A	8F042SAB	0/45
TSMC 0.35u	Z8F022APB020SG	AACFN043.00QQQA.A	8F042SAB	0/45
AMKOR				
TSMC 0.35u	Z16F2811AL20EG	ABCAF897.00QRC	8F1285AB	0/45
TSMC 0.35u	Z8F0411PH020SG	ABCCY982.00IPA	Z8F082BE	0/45
GREATEK				
X4120	Z84C0010AEG	AGT75258QPC	Z84C00HB	0/45
X4120	Z84C0006PEG	AGT75258PE	Z84C00HB	0/45
NANTONG				
0.13um, 2P 5M	S3F8S19XZZ-ER89	603Y8Y5	S3F8S19XZZ-W0WY	0/45
PSTS				
0.13um, 2P 5M	S3F80RBXZZ-KZ8B-2249	A66514804B	S3F80RBAA	0/45
0.13um, 2P 5M	S3F8S6BXZZ-QT8B	603UPP105	S3F8S6BXZZ-W0WB	1/45
0.13um, 2P 5M	S3F8S7BXZZ-TW8B	603T9Y405	S3F8S7BXZZ-W0WZ	0/45

Table 4-7
C-Mode Scanning Acoustic Microscope Monitor

CSAM MONITOR				
ASSY LOC	**DEVICE**	**LOT #**	**SAMPLE SELECTION**	**RESULT**
AMKOR				
TSMC 0.35u	Z16F2811AL20EG	ABCAF897.00QRC	Pre-MSL 3	0/22
TSMC 0.35u	Z16F2811AL20EG	ABCAF897.00QRC	Post MSL 3	0/22
X5221	Z86E8316VEG	ABT66209HQQQQQPA	Pre-MSL 3	0/22
X5221	Z86E8316VEG	ABT66209HQQQQQPA	Post MSL 3	0/22
UNISEM-BATAM				
X5221	Z8927320VSG	AAT74867HS.A	FRESH	0/22
X5221	Z8927320VSG	AAT74867HS.A	POST MSL 3	0/22
X5220	Z86E4412ASK	AEAT75256HPQQ2.A	FRESH	0//22
X5220	Z86E4412ASG	AEAT75256HPQQ1.A	FRESH	0/22
X5220	Z86E4412ASK	AEAT75256HPQQ2.A	POST MSL 3	0//22
X5220	Z86E4412ASG	AEAT75256HPQQ1.A	POST MSL 3	0/22
X5220	Z86E4412ASK	AEAT75256HPQQ2.A	post 1000xTC	0/5
X4120	Z16C0210VSG	AT80215A.A	Pre-MSL 3	0/22
X4120	Z16C0210VSG	AT80215A.A	Post MSL 3	0/22
TSMC 0.35u	Z8FS040BSB20EG	AACGF295.00G.A	Pre-MSL 1	0/22
TSMC 0.35u	Z8FS040BSB20EG	AACGF295.00G.A	Post MSL 1	0/22
X3120	Z84C2006VEG	AAT69318QPAA.A	Pre-MSL 3	0/22
X3120	Z84C2006VEG	AAT69318QPAA.A	Post MSL 3	0/22

CHAPTER 5

Package & Test Information

Zilog products are assembled and tested by qualified subcontractors using their standard procedures and approved by Zilog. Package types , material and test requirements including handling and storage of surface mounted devices, reflow conditions, thermal characteristics and ROHS compliance for Zilog products are defined below.

Package and Test Information

Package types

8 / 18 / 20 / 28 / 40 / 48	Plastic Dual In-line Package (PDIP)
42 / 52 / 64	Shrink Dual In-line Package (SDIP)
28 / 44 / 68 / 84	Plastic-Leaded Chip Carrier (PLCC)
80 / 100 /144	Quad Flat Pack (QFP)
32 / 44 / 64 / 100 / 144	Low Profile Quad Flat Pack (LQFP)
8 / 18 / 20 / 28	Small Outline Integrated Circuit (SOIC)
20 / 28 / 48	Shrink Small Outline Package (SSOP)
144 / 256	Ball Grid Array (BGA)
8 / 20 / 28 / 32 /44	Quad Flat No-leads (QFN)

Technology Data:

Die attach (method/composition)	Oven cure/silver filled epoxy
Wirebond (type/material)	Ball bond, thermosonic/gold to aluminum Crescent bond, thermosonic/gold to silver plated frame
Bonding wires (material/diameter)	Gold 1.0 / 1.3 mil
Package seal	Transfer epoxy molding
Lead finish	Solder plate or Pure Tin (Green Product)
Leadframe material/plating	Copper (A151) / Ag spot plate for PLCC Copper (A194)/Ag spot plate for PDIP, SDIP, SOIC and SSOP Copper (A7025)/Ag spot plate for QFP and VQFP
Leadframe plating thickness	Ag spot is 150-400 micro-inches
Moisture Sensitivity Level for Surface Mount Devices	PLCC, QFP, LQFP, QFN & LBGA: MSL = 3, Floor Life = 168 hrs. @ 30°C/60% RH. PDIP, SSOP and SOIC are not moisture sensitive.

Pre/Post Packaging Device Test Procedures

Type of Testers	Sentry 15, Megatest, ITS9000, Teradyne J750, and Nextest
Provision for Testing at Speed	Yes
Provision of high temp testing	Environmental handlers
Provisions for tape and reel shipment of SMT devices	Yes
Provisions for tray shipment of QFP devices	Yes

Reduction of Hazardous Substances (RoHS)

In September of 2003, Zilog began offering a 'Green' product version of our integrated circuits that is both lead-free and RoHS compliant. The customer must specify the Green product version because we offer both our standard (Sn/Pb solder plate) and Green product versions concurrently.

What Does Lead-Free/RoHS Compliant Mean?

Reduction of Hazardous Substances (R0HS) Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 restricts the acceptable levels of the following six substances listed in Table 1.

TABLE 1

Substance	Symbol	Acceptable Concentration
Lead	Pb	<1000 ppm
Cadmium	Cd	<100 ppm
Mercury	Hg	<1000 ppm
Hexavalnet Chromium	Cr[VI]	<1000 ppm
Polybrominated Biphenyls	PBB	<1000 ppm
Polybrominated Diphenyl Ethers including DecaBDE	PBDE	<1000 ppm

All fabrication and assembly of Zilog products is provided by qualified subcontractors. Zilog requires that all suppliers who provide green product versions certify that they are in compliance with the restrictions contained in Table 1. Zilog has achieved RoHS compliance through the use of encapsulants that do not contain antimony or bromine-based flame retardants and by offering a lead-free 100% matte tin termination plating.

Unique Part Numbers

We identify our Green products with a unique Zilog Product Specification Index (PSI) environment code "G" for Green packages (for example, Z84C0008FEC becomes Z84C0008FEG and Z8F0822SJ020SC becomes Z8F0822SJ020SG). Therefore, any Green Zilog product version, with the exception of those using custom top-marks, can be immediately identified by its top mark.

SMT Reflow Profiles

We use the widely accepted tin/silver/copper (SnAgCu) alloy of SN3.9Ag0.6Cu solder paste because of its lower melting temperature (217°) and long-term reliability. The SnAgCu requires higher reflow temperatures, so SMT processes must be optimized to achieve the best yields and reliability. Zilog packages are classified per JEDEC J-STD-020 as MSL Level 3.

Table 2 describes the profiles of tin-lead and lead-free assemblies.

TABLE 2

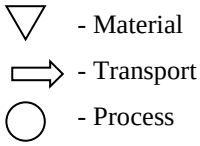
Recommended Reflow Profile	**Tin-Lead Assembly**	**Lead-Free Assembly**
Preheat		
Temperature Minimum (Tsmin)	100°C	150°C
Temperature Maximum (Tsmax)	150°C	200°C
Time (minimum to maximum)	60–120 seconds	60–180 seconds
Tsmax to TL ramp-up rate	3°C per second, max	3°C per second, max
Time maintained above:		
Temperature (TL)	183°C	217°C
Time (tL)	60–120 seconds	60–120 seconds
Peak Temperature (TP)	220-225°C	260°C max
Time within 5° of Peak Tp	10–30 seconds	20–40 seconds
Ramp-down Rate	6°C per second max	6°C per second max
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

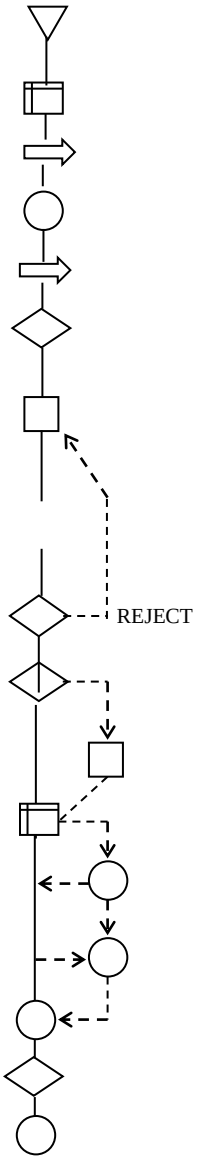
Note: (Based on AN0161 Revision 4)

1. All temperatures refer to the top side of the package, measured on the package body surface.
2. It is not recommended that tin-lead product be used with the lead-free solder reflow profile.

PLASTICS PROCESS FLOW

Legend:



Flow	***Process/Item***	***Document***
	Wafer	
	Die Bank	SOP2139
	Pack/transport to Subcon	SOP1594
	Subcon Assembly	
	Pack/transport ZEPI	SOP1594
	Incoming Inspection of Subcontract Zilog Products	SOP1650
	Electrical Test	Subcontractor Applicable Specs
	<For Stress Test D Flow only> Burn-In (48hrs or as specified on PSI)/ 100% Electrical Test at Room	SOP1638 Subcontractor Applicable Specs
	Electrical Test Gate	
	QC Outgoing & Shipping Gate	
	Final Visual Inspection (For visual reject)	SOP1619
	Finished Goods	
	Bake Out (for LQFP/QFP/TQFP)	SOP1657
	Tape & Reel (as required per PSI)	SOP1665
	Pack	SOP1618
	Shipping Audit	SOP1670
	Ship	SOP1670

PLASTIC-STANDARD ASSEMBLY/TEST PROCESS

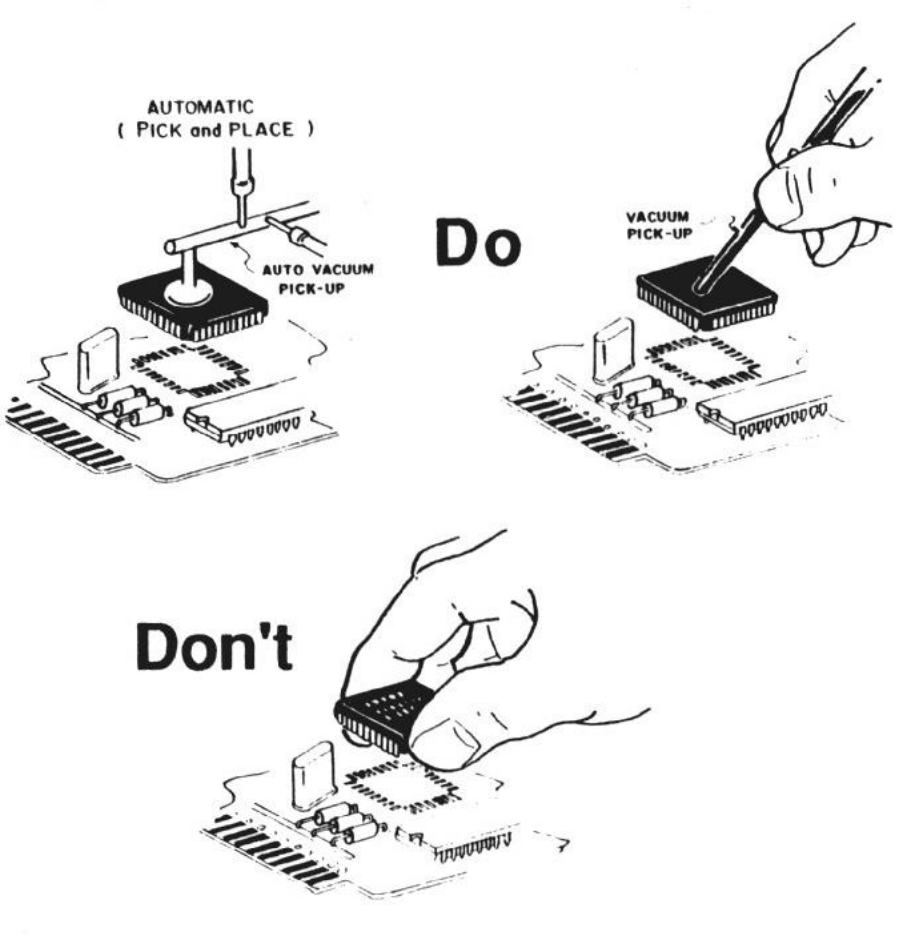
PLASTIC – STANDARD (C FLOW)
• DIE BANK
• WAFER SAW
• EPOXY DIE ATTACH
• WIREBOND
• MOLD
• STRIPMARK
• SOLDER PLATE
• BAKEOUT (FOR PLCC)
• TRIM/FORM
• 100% ELECTRICAL TEST – HOT AND QC SAMPLE ELECTRICAL AT 25ºC
• QC PRESHIP INSPECTION
• BAKEOUT FOR QFP/VQFP IN TRAY
• TAPE AND REEL (OPTIONAL FOR SOIC, QFP AND PLCC)
• PACK

PLASTIC – STRESSED (D FLOW)
• DIE BANK
• WAFER SAW
• EPOXY DIE ATTACH
• WIREBOND
• MOLD
• STRIPMARK
• SOLDER PLATE
• BAKEOUT (FOR PLCC)
• TRIM/FORM
• 100% ELECTRICAL TEST – HOT
• BURN-IN 48 HOURS AT 125ºC
• 100% ELECTRICAL TEST AT ROOM
• QC PRESHIP INSPECTION
• BAKEOUT FOR QFP/LQFP IN TRAY
• TAPE AND REEL (OPTIONAL FOR PLCC, QFP, SOIC)
• PACK

The Handling and Storage of Surface Mount Devices

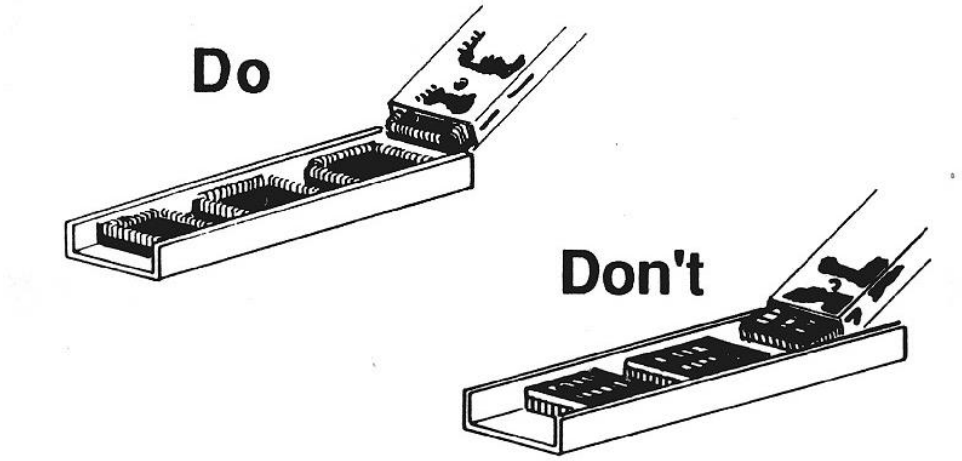
1. Handling

Components should be handled with vacuum pick to ensure that coplanarity of leads is maintained.



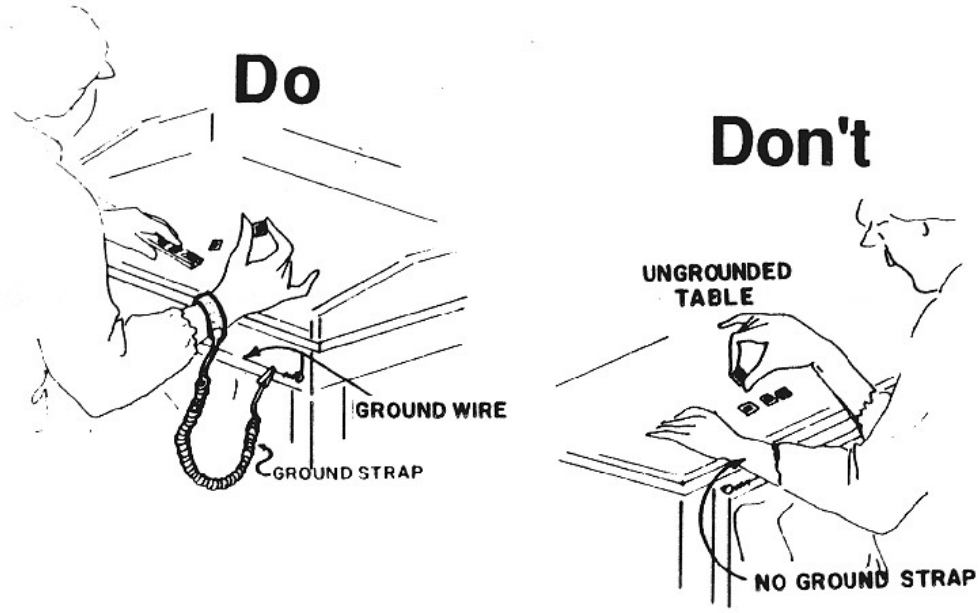
2. Lead Protection

Avoid sliding of units with leads in contact. The solder coating is prone to contamination/scraping. If sliding cannot be avoided, the contact surface should be clean and smooth.



3. ESD Protection

Observe ESD protection at all times. *These are static sensitive devices.*



4. Storage/Unpacking Caution

The plastic body of a surface mount product may be subjected to high temperatures during the printed circuit board assembly operation. Any moisture that may be present in the plastic may expand and damage the unit. Therefore, it is very important that the surface mount IC be dry before the printed circuit board operation begins.

Zilog assures that the unit is thoroughly dry before final packing for shipment. The units are shipped in a "dry pack" envelope designed to keep moisture away from the IC's. The user should carefully observe the following practices to assure that the units remain moisture free at the time of the printed circuit board soldering operation:

- Do not open the dry pack until you are ready to solder. Product may be exposed to ambient conditions of 30C/60%RH (or less) for no more than 168 hours ***This corresponds to a moisture sensitivity level of 3.***
- Unopened dry packs may be stored at <40°C/90% RH.
- When the dry pack must be opened for a short period of time (such as for incoming inspection), it should be resealed as soon as possible, ensuring that the desiccant remains inside the dry pack. Resealing should be done with heat seal for best closure of the bag.
- If the units have exceeded their exposure time or if the humidity indicator card in the bag is beyond requirement, devices should be baked before board soldering at procedures defined on J-STD-033. Product supplied in Tape and Reel must be removed from the Tape and Reel and placed in heat
  resistant trays prior to baking.
- Die Sales – Wafers and plated dice are kept in CDA cabinet with max RH of 35%, temp of 16-27 degrees C (60-80.6 deg F).

5. Soldering

Recommended surface mount profile for standard tin/lead solder plate is as follows:

* Maximum 3°C/sec. ramp up.
* Maximum 220°C peak temp.
* Minimum 1 min. cool down from peak temp. to 50°C.

Please refer to our Lead-Free products FAQ on http://www.zilog.com lead-free soldering recommendations.

6. Desoldering

Parts removed due to board assembly problems or suspected failure.
If boxed-in type desoldering fixture is used, the following are recommended operating parameters:

* Package Temp: 220°C max.
* Dwell Time: 1 min. max.

It is important that the above precautions are followed to ensure integrity of the packages.

THERMAL CHARACTERISTICS

Calculation of Device Junction Temperature

Failure rates and Failures in Time (FITS) obtained from life test data are based on junction temperature (TJ). Junction temperature is more accurate than ambient temperature since it considers power dissipation and thermal impedance as well. Junction Temperature (TJ) is incorporated into the Arrhenius Equation for accelerated failure rates by using the following equations.

Junction Temp. (T_J): $T_J = (\theta_{JA})\ (P_D) + T_A$

where: θ_{JA} is the thermal resistance of junction with respect to ambient (C/W). P_D is the maximum power dissipation at T_A in watts

and: T_A is the ambient temperature °C.

Case Temperature (T_C): $T_C = T_J - (\theta_{JC})\ (P_D)$

where: θ_{JC} is the thermal resistance of junction with respect to case.

Illustration: In order to calculate junction temperature (T_J) and case temperature (T_C) for static airflow for the Z86C04 in an 18L PDIP, we do the following:

1. At 25°C, maximum power dissipation for this device is 0.08 watts.

2. For our example, ambient temperature is denoted by T_A and is assumed to be 25°C.

For the Z86C04 in plastic (copper); θ_{JA} and θ_{JC} are 75 and 18°C/watt respectively.

Therefore, $T_J = 75 \times (0.08) + 25 = 31.2°C$, and

$T_C = 31.2 - (18 \times 0.08) = 29.8°C$

Table 5-1. Device θ_{JA}, θ_{JC} Table Summary Of Thermal Characteristics For Zilog Plastic Packages

Package Type	*Package Code*	θ_{JA}	θ_{JC}	*Lead Frame*
PDIP	**P**			
18L		75	18	Cu
20L		75	18	Cu
28L		60	12	Cu
40L		43	12	Cu
42L		42	11	Cu
48L		40	8	Cu
52L		38	8	Cu
64L		42	14	Cu
PLCC	**V**			
44L		46	13	Cu
68L		43	14	Cu
84L		42	12	Cu
QFP	**F**			
44L		45	10	Cu
80L		43	16	Cu
100L		38	17	Cu
LQFP	**A**			
64L		70	19	Cu
100L		40	25	Cu
SOIC	**S**			
8L		110	N/A	
18L		70	N/A	Cu
20L		75	N/A	Cu
28L		60	N/A	Cu
SSOP	**H**			
20L		75	18	Cu
28L		60	12	Cu
48L		45	12	Cu

Notes: **P**=Plastic DIP
V=PLCC-Plastic Leaded Chip Carrier
F=QFP-Plastic Quad Flat Pack
A=LQFP-Low Profile Quad Flat Pack
S=SOIC-Small Outline Integrated Circuit
N=BGA- Ball Grid Array
HZ = SSOP **–** Small Shrink Outline Package

CHAPTER 6

Quality Systems

Quality Systems

QUALITY SYSTEMS

- Organization: Quality control departments are located at Zilog worldwide headquarters in Milpitas, CA, Zilog Idaho Technology Center in Meridian, ID and Zilog Electronics Philippines (ZEPI) in Manila, PI.

- Equipment: Idaho and Manila can conduct material analysis on failures including decapsulation, SEM, microprobe, Emission microscope, X-Ray, EDX, and cross-section. See Table 2-2 for a complete list of QC test equipment.

WAFER FOUNDRY: 100% of wafer manufacturing is subcontracted .

ASSEMBLY SUBCONTRACTORS: 100% of assembly is subcontracted.

LOT TRACEABILITY: Lot traceability is provided by product date code and lot code that is incorporated into the standard Zilog integrated circuit device topmark.

AVAILABILITY OF DOCUMENTATION ON MONITORING: Documents are available in either hard copy or electronic form .

QUALITY DATA:

Data availability: Outgoing quality is measured by the quality control acceptance/rejection data and on each production lot which is reported on a PPM basis.

TESTING (QA/Operating)

- Test program release procedure: Zilog has a formal test program review/release procedure, per Procedures SOP2156.
- Does QA sample test? Yes. Lots are sampled by QA using a statistically valid sampling plan. If the QA sample fails, the entire lot is re-tested and a second QA sample is drawn.
- Is datasheet tested or guaranteed? Zilog provides its product specifications to the customer in a document called a data sheet. The product specification describes the attributes that Zilog warrants.
- Is the product tested at full temperature range? Yes
- Is the product 100% electrically tested prior to QA? Yes
- Does QA pull samples for both AC and DC Testing? Yes
- How is propagation delay tested (e.g., simultaneous switching effect): Simultaneous
- Fault coverage (Operating vs. QA): As close to 100% as practical
- Coplanarity requirement on SMD: 4 mils maximum; reference the seating plane
- Define failure: Does not meet specifications

TEST TAPE SUPPORT: Test tapes, load boards and documentation are available

WHAT HAPPENS WHEN FAILURES OCCUR?

- Is sample truncated? No
- Corrective action plan: Failure analysis is initiated by R/QA
- How is product segregated (i.e., is there protection from mixing)? Automatic binning during electrical test is used to segregate product. Product traceability to the customer order is maintained by a unique part numbering system (SOP0902)

WHEN PROCESSES ARE PERFORMED OFFSHORE, WHAT ARE THE CONTROLS?:
Same as onshore; the Manila plant is monitored by the on-site QA organization. Periodic audits are performed on all offshore facilities by Zilog personnel.

AVAILABILITY OF PROGRAMMING FACILITIES:
Zilog develops its own test programs with facilities located in Manila, PI, Milpitas, CA and Meridian, ID.

QA AUDIT:

- Availability of audit reports: Serialized run sheets and audit checklists are maintained by the Quality Control organization.

DOCUMENT CONTROL SYSTEM

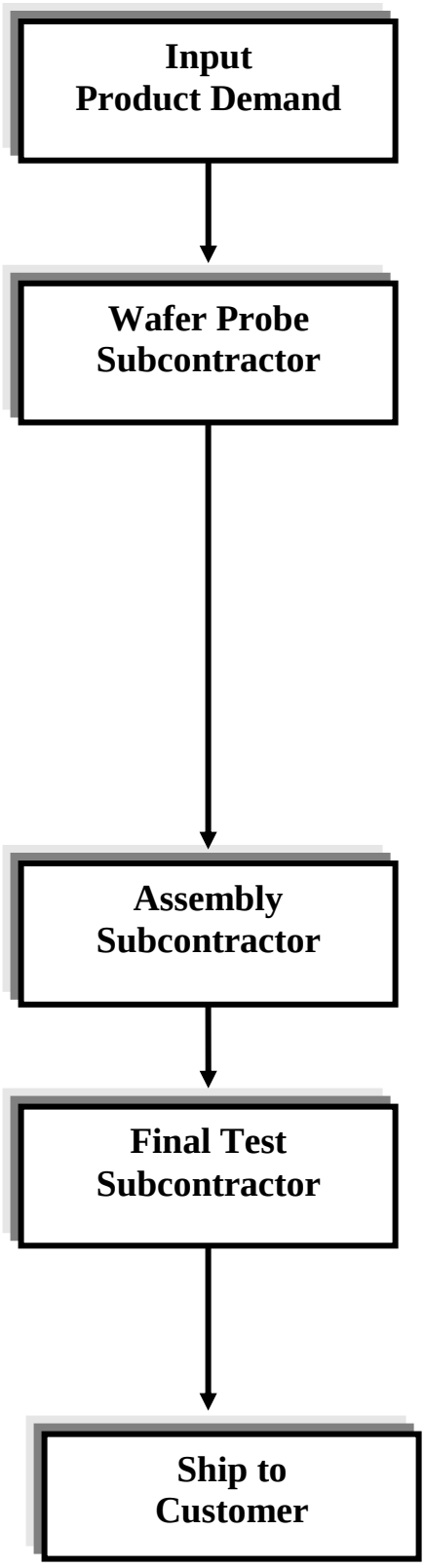
Zilog's Document Control Department promotes reliability and quality through efficient, global document management and revision control systems. The Document Control Department maintains an electronic document management system that is accessible by Zilog employees worldwide 24 hours a day. Manufacturing documents are available electronically for all wafer foundry and assembly subcontractors. The system automatically manages revision control; ensuring users have the most up-to-date version every time.

"Zilog Document Control oversees the worldwide document management processes for revision controlled documents. They are also responsible for managing design, engineering and marketing documents and records as well as company-wide policies and procedures submitted to Zidoc."

Additional details regarding any of the sections contained in this document may be found in Zilog policies, procedures or specifications. General categories are listed below. Please contact the Zilog Director of Quality and Reliability with specific questions.

- Corporate-Wide Policies
- Standard Operating Procedures for Business Units, Corporate Communications, Finance, Human Resources, Information Technology, Legal, Operations, Reliability and QA, Sales, Strategy, Technology, Design & Test
- Core Process Documents for all Phases of the Product Life Cycle
- Product and Process Specific Manufacturing, Assembly and Test Procedures and Specifications

Flow Chart


Input
Product Demand
Wafer Probe
Subcontractor
Assembly
Subcontractor
Final Test
Subcontractor
Ship to
Customer

CHAPTER 7

Quality and Reliability Glossary

Quality and Reliability Glossary

TERM	DEFINITION
Å:	Symbol for Angstrom, which equals 10^{-10} meters (one ten-billionth of a meter).
Accelerated Life Test:	A life test, in which the applied stress level exceeds that needed in actual use in order to shorten the time required to observe failure. A good accelerated test should not alter the basic modes and/or mechanisms of failure.
Acceleration Factor:	The ratio of the times needed to obtain the same failure rates under two different sets of stress conditions involving the same failure modes or mechanisms.
Activation Energy (Ae):	The energy level needed to activate a specific failure mechanism.
AES:	Auger Electron Spectroscopy typically used for interlayer dielectrics and passivation films.
Align:	The operation of exposing a resist covered wafer in a projection printer.
APCVD:	Atmospheric Pressure Chemical Vapor Deposition. One method for deposition of glass used for interlayer or passivation dielectric.
ASSP:	Application Specific Standard Product.
AQL:	Acceptable Quality Level. Generally, 95 percent confidence that material of the stated AQL will pass sample inspection.
Bonding:	The act of connecting package leads to specified locations on the chip via fine wire.
Bond Pads:	Exposed aluminum pads on a chip to which wires from the package lead frame are bonded during assembly.
Burn-In:	The operation of a device prior to its application, at elevated temperature and/or voltage for a specific period of time. The purpose is to stabilize the device characteristics, identify early

TERM	DEFINITION
	failures, and eliminate devices subject to infant mortality or excessive parametric drift.
BPSG:	Boron doped Phosphosilicate Glass.
CD:	Critical Dimension.
CFA:	Customer Failure Analysis/Correlation Request.
C of C:	Certificate of Conformance.
CMOS:	Complementary MOS technology combining n and p transistors in the same product. Advantages include low power dissipation.
Confidence:	A specialized statistical term which refers to the probability of a statement being true.
Check:	A visual check done at the conclusion of a (dry or wet) masking step.
Chip:	One square on a wafer containing a single integrated circuit. The substrate on which all active and passive components of a circuit are fabricated; also called a die.
Clean Room:	The room in a chip fabrication plant in which wafers are processed. This area features a controlled environment with filtered air that eliminates essentially all dust and dirt.
Contact:	A connection between two conductive layers, e.g., metal-to-silicon contact.
Control limit:	A statistically defined limit which determines whether or not a process has changed significantly as compared to past history. A measure of statistical process control.
C-SAM:	C-Mode Scanning Acoustic Microscope which examines packaged units and produces high resolution, ultrasonic images.
CVD:	Chemical Vapor Deposition of thin films. Gaseous reactants are brought together over the silicon wafer, depositing required layers typically used for interlayer dielectrics and passivation films.
DC:	Document Control.
DESC:	Defense Electronic Supply Center.
DI:	Deionized water.
DIP:	Dual-in-Line Package.
DRC:	Design Rule Check.
DUT:	Device Under Test.
Depletion transistor:	A MOSFET with a permanently “on” channel; requires a negative

TERM	DEFINITION
	applied gate voltage to turn off (see “enhancement transistor”).
Develop:	A chemical process that solidifies photoresist where it has been exposed and removes it elsewhere (for negative resist) or vice versa (for positive resist).
Develop inspect:	A visual check following dry masking to verify proper resist patterning before etch, e.g., alignment and thickness are checked.
Die:	A single integrated circuit separated from the wafer on which it was made; also called a chip.
Diffusion:	The process of doping silicon by diffusing impurities from the surface into the wafer at high temperature. Any region in the silicon substrate doped by diffusion or by ion implant (e.g., source and drain diffusions).
Dopant:	Any impurity intentionally introduced into silicon to control its electronic behavior (e.g., Boron, Arsenic, and Phosphorus).
Dose:	In ion implant, a measure of the amount of dopant implanted; usually expressed in ions per square centimeter.
Drain:	A highly doped region adjacent to a transistor currently carrying channel. It carries electrons out of the transistor to the next circuit element or conductor.
Dry Masking:	A process segment where a photoresist is spun onto the wafer, soft baked, exposed, and developed to obtain a desired pattern ready for etch or implant (see "wet masking”).
EDMS	Electronic Data Management System
EDX:	Energy Dispersive X-ray analysis. Normally uses electron beam excitation in the scanning electron microscope.
EOS:	Electrical overstress, common application failure mechanism.
ESD:	Electrostatic discharge, common handling failure mechanism.
Enhancement transistor:	A MOSFET with a normally “off” channel; requires a positive applied gate voltage to turn on (see “depletion transistor”).
Etch rate:	The rate at which a given layer is etched off in a given standard acid solution, expressed in Å/sec.
Evaporation:	Deposition technique for Aluminum, Gold, and Chromium thin films.
Expose:	Expose a photoresist-coated wafer to light through a mask.
FAE:	Field Application Engineer.
Final Test:	Measurement of assembled device performance. Products are

TERM	DEFINITION
	categorized by speed/power/performance criteria.
FIT:	"Failure units" or "Failure in Time," a measure of failure rate defined as one failure in 10^9, or one billion device hours.
FPO:	Finish Process Order. A lot traveler that accompanies each lot through the finish (Mark and Pack and FQA) areas.
FQE:	Field Quality Engineer.
Gate:	The gate of a transistor.
Gate oxide:	Dielectric oxide between the gate and the channel region of a transistor.
Generic:	Devices similar in process or function. Zilog uses a generic approach in its Reliability Program. Devices built in the same wafer fab process and having similar complexity or function are grouped into a "generic" product family. Data on any device within a family is considered indicative of the performance of all other devices in that group and process line.
Gettering:	Trapping of contamination atoms (especially alkali ions) to prevent their drift into device regions where they may affect electrical performance.
Glass:	The amorphous form of SiO_2, used in various insulating layers on the wafer.
Hard Bake:	A step following dry masking, where the resist is heated to prepare it for wet etch.
HAST:	Highly Accelerated Stress Test.
HTOL:	High Temperature Operating Life.
IC:	Integrated Circuit.
Infant Mortality:	Initial failure rate in life studies. It is followed by the early failure period and then the final wear out period of failure (bathtub curve).
IQC:	Incoming Quality Control.
K:	Kilo, thousand, 10^3.
Layout:	A magnified, physical representation of an electronic circuit at the transistor level.
LCC:	Leadless Chip Carrier.
Lead:	The external connection to a packaged integrated circuit.
Life Test:	A test for the purpose of estimating some characteristic(s) of a device's useful lifetime.

TERM	DEFINITION
LSI:	Large Scale Integration
LPCVD:	Low Pressure Chemical Vapor Deposition. Typical method for deposition of glass used for interlayer or passivation dielectric.
LTO glass:	Low Temperature Oxide glass used for interlayer or passivation dielectric. Typically deposited at the same temperature as APCVD deposited glasses used for passivation, but at low pressure.
LTPD:	Lot Tolerance Percent Defective. A sample plan that will reject 90 percent of the lots equal to or worse than the stated LTPD value.
Mask:	A pattern usually "printed" on glass, used to define areas of the chip on the wafer for production purposes.
Masking:	The lithography portion of the process or physical area where lithography occurs.
MeV:	Million electron Volts.
meV:	Milli electron Volts.
MFG:	Manufacturing.
Mil:	0.001 inch.
MIL:	Military.
MOS:	Metal Oxide Semiconductor integrated circuit technology.
MSL	Moisture Sensitivity Level.
MRB:	Material Review Board.
MTBF:	Mean Time Between Failures.
MTTF:	Mean Time to Fail. Time to 50 percent Cumulative Fail.
Nano:	10^{-9}.
Negative photoresist:	A resist material in which unexposed areas are developed away.
NIST:	National Institute of Standards and Technology.
Nitride:	Silicon Nitride, Si_3N_4.
NMOS:	N channel MOS technology.
Nm:	Nanometer (1nm = 10A = 10^{-9} meters).
Ns:	Nanoseconds (10^{-9} seconds).
OEM:	Original Equipment Manufacturer.
OTP:	One Time Programmable Product sold in plastic packaging. No window is provided for UV erasure.
"Oxi":	A process whereby thick oxide islands are grown between active

TERM	DEFINITION
	device regions for better isolation and performance.
Oxynitride:	A plasma deposited passivation or interlayer dielectric film consisting of silicon, oxygen, and nitrogen.
P:	Phosphorous.
PDIP:	Plastic Dual In-Line Package.
PE:	Product Engineer.
PECVD:	Plasma Enhanced Chemical Vapor Deposition.
PGA:	Pin Grid Array (package).
PLCC:	Plastic Leaded Chip Carriers.
PM:	Procedural Manual that contains Zilog's policies and procedures.
POA:	Point of Acceptance.
PPM:	PPM Quality Data, Parts per Million defective; 1000 PPM = 0.1 percent defective.
PPOT:	Pressure Pot.
PROM:	Programmable Read Only Memory.
PSG:	Phosphosilicate Glass. A glass containing phosphorus (in the form of P_20_5). LTO, Pyrox and Pyroglass are all types of PSG.
Package:	The container used to hold an active semiconductor device.
Photolithography:	The portion of the process involving the use of light sensitive photoresist material for layer definition.
Photomask:	(1) A patterned chrome on glass photographic plate used to transfer a pattern to photo-resist in dry masking. (2) A process segment involving the patterning of a given layer by use of a photomask.
Photoresist:	A light sensitive polymer material that is used as a mask for etching and ion implant steps. See also Negative and Positive Photoresist.
Plasma ash:	A process using a gas transformed by an RF field into a reactive plasma.
Plasma deposition:	Deposition of thin films using gaseous reactants in the presence of a plasma for lower temperatures.
Plasma etch:	An etching process using a gas transformed by an RF field into a reactive plasma.
Poly:	Polycrystalline silicon made up of many tiny crystals (as opposed to single crystal silicon.

TERM	DEFINITION
Poly Re-ox:	Oxidation of the poly after it has been defined. The re-ox provides the interpoly di-electric in a double (two layer) poly process.
Positive photoresist:	A photosensitive organic polymer material in which exposed areas are developed away.
Prebake:	First step of dry masking, in which the wafers are dried in an oven prior to resist application.
Probe:	The first electrical test of processed wafers.
Process Templating:	The profile displayed by the process evaluation parameters, which are automatically recorded from the test patterns on wafers as they proceed through the production line.
Projection Aligner:	A machine that projects the photomask onto the resist-coated wafer. The mask is the same size as the wafer and imaged 1:1 on the wafer.
Pyrox:	A type of phosphosilicate glass containing approximately 4.5 wt Phosphorous.
QA:	Quality Assurance.
QE:	Quality Engineer.
QR-XXXX:	Product or Process Qualification Report (XXXX = report number).
RBS:	Rutherford Back Scattering. A method for non-destructive depth profile analysis of thin films by back scattering of high-energy helium ions.
RE:	Reliability Engineer.
RGA:	Residual Gas Analysis.
ROHS	Restrictions on Hazardous Substances
QFP:	Quad Flat Package.
QIP:	Quality Improvement Process.
Q&R:	Quality and Reliability.
RH:	Relative Humidity.
RIE:	Reactive Ion Etch.
RMA:	Return Material Authorization.
ROM:	Read Only Memory.

TERM	DEFINITION
Refractive Index:	A basic physical property which determines the extent of light bending (refraction) upon entering the surface. Used in thin film process control as an indirect measure of chemistry.
Resist:	See Photoresist.
SDE:	Statistical Design of Experiments.
SEM:	Scanning Electron Microscope. A microscope which makes use of a scanning beam of electrons to image detail less than 100A in size (surface only).
SIMS:	Secondary Ion Mass Spectroscopy.
SL-Lot:	Special Lot. Zilog identification used to identify products designed to unique customer requirements.
SPC:	Statistical Process Control.
STS:	Ship-to-Stock. Eliminates need for customer IQC.
Silicon:	Metallic element which forms the substrate in most semiconductor devices.
Soft bake:	A step preparing freshly spun photoresist for exposure by baking it in an oven (to remove excess solvent).
SOIC:	Small Outline Integrated Circuit package.
Source:	Equivalent to the drain of a transistor with the exception that electrons leave the source into the channel of the active device.
Spec. Limit:	Absolute acceptable limit for a process parameter.
Spin:	A process step which coats a spinning wafer with liquid photoresist by dispensing the liquid onto its center.
Sputtering:	Deposition of a metal layer by bombarding a metal target with heavy ions from a gaseous (e.g., argon) plasma. Metal atoms are removed from the target and deposited onto the wafer during this process.
TD:	Technology Development.
TDDB:	Time Dependent Dielectric Breakdown.
TEM:	Transmission Electron Microscope. A microscope used to obtain high-resolution images with a transmitted electron beam by electron lens imaging rather than scanning.
THB:	Temperature Humidity Bias (85°C/85% RH).
TSOP:	Thin small outline package.
Test patterns:	Special electrical test structures included on production device

TERM	DEFINITION
	wafers for monitoring critical parameters.
Thermal oxide:	A high quality Si_{O2} layer grown by oxidizing the silicon in a furnace (as opposed to externally deposited glass).
UL:	Underwriters Laboratory.
UV:	Ultra Violet.
V/I:	A monitor measuring voltage and current between probes applied to a semiconductor layer. Measures layer resistivity.
Visual:	A check of process quality by examination of wafers under a light microscope.
VLSI:	Very Large Scale Integration.
VQFP:	Very small Quad Flat Pack package.
Vt:	Transistor threshold voltage. Voltage at which the transistor turns on.
Wafer:	A thin piece of silicon sliced from a cylinder shaped crystal. It is polished so that the surface is like a mirror. It is most commonly found in 4, 5, and 6-inch diameters. The wafer is the base material for most of the world's integrated circuits.
Wafer flat:	A flat area ground onto the original silicon ingot from which the wafers are sliced. Gives crystallographic orientation.
Waterfall Guardbanding:	The technique of testing a circuit at different levels of the manufacturing process, to insure above marginal product performance and compliance.
Wet masking:	Process segment following "dry masking" in which the wafer, covered with the resist pattern, is etched to transfer the resist pattern to the wafer. The resist is then removed (includes wet and/or plasma etching).
Wet etch:	Etching in a liquid acid or solution.
Wire bonding:	The process of connecting thin wires from the chip's bond pads to the package lead. (This is done at assembly.)
ZD:	Zero Defects.
ZEPI:	Zilog Electronics Philippines, Inc.
ZUS:	Zilog Corporate Headquarters, Milpitas, California.